IN THE CLAIMS:

Please amend claim 1, as follows:

1. (Currently Amended) A system LSI comprising:

a group of external terminals to which a plurality of external devices can be connected;

a processor carrying out computation and control on the basis of programs;

a bus interface specifying an external device which is to be an object of access from among the plurality of external devices on the basis of a control signal outputted from the processor, and outputting access time data instructing an access time to said external device and a request signal requesting access to said external device;

a register storing the access time data outputted from the bus interface;

an input terminal to which is inputted, from an exterior, a wait signal which designates extension of the access time to said external device; and

an external bus controller which, in accordance with the access time data stored in the register and the request signal outputted from the bus interface, accesses said external device via the group of external terminals, and extends the access time to said external device in accordance with the wait signal inputted to the input terminal,

wherein the external bus controller extends the access time to said external device in units of the access time which the access time data instructs.

2. (Cancelled)

3. (Original) The system LSI of claim 2, wherein the external bus controller extends the access time to said external device by adding one of or a plurality of the access times to the access time which the access time data instructs.

4. (Original) The system LSI of claim 1, wherein the external bus controller extends the access time by extending a time in which an address of said external device is outputted to said external device.

5. (Original) The system LSI of claim 1, wherein the external bus controller

extends the access time by extending a time in which a selection signal, which instructs that said external device be selected, is outputted to said external device.

6. (Original) A system LSI having a processor successively reading programs and carrying out computation and control; a bus interface specifying an external device which is to be an object of access on the basis of a control signal outputted from the processor; an access control register setting an access extension time with respect to said external device; and an external bus controller carrying out reading and writing of data between the bus interface and said external device in accordance with the access extension time,

wherein the system LSI comprises a wait signal generating section which, on the basis of a control signal outputted from the processor, generates a wait signal which designates extension of an access time to said external device, and the external bus controller extends the access time to said external device in accordance with the wait signal.

7. (Original) A system LSI having a processor successively reading programs and carrying out computation and control; a bus interface specifying, on the basis of a control signal outputted from the processor, one of an external device which is to be an object of access and an external device which is to output a wait signal; an access control register setting an access extension time with respect to said external device; and an external bus controller carrying out reading and writing of data between the bus interface and said external device in accordance with one of the extension time and the wait signal,

wherein the system LSI comprises a re-map signal generating section which, on the basis of a control signal outputted from the processor, generates a re-map signal, and the control signal specifies said external device when the re-map signal is supplied to the bus interface.

8. (Original) The system LSI of claim 6 , wherein the external bus controller extends the access time to said external device by adding one of or a plurality of access times to an access time corresponding to the wait signal.

9. (Original) The system LSI of claim 6, wherein the external bus controller

extends the access time by extending a time in which an address of said external device is outputted to said external device.

10. (Original) The system LSI of claim 6, wherein the external bus controller extends the access time by extending a time in which a selection signal, which instructs that said external device be selected, is outputted to said external device.